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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,879	08/22/2003	Hin-Kwai Lee	NM-103	1878

23933 7590 01/16/2007

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/604,879	LEE, HIN-KWAI	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14 and 16-20* is/are rejected.

7)☒ Claim(s) *7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Response to Arguments

2. In view of the Applicant's amendment submitted 12 October 2006, the **35 U.S.C. 112 rejections of claims 1 and 9 and the 35 U.S.C. 101 rejections of claims 9-20 have been withdrawn.**

3. Applicant's arguments, see page 9, filed 12 October 2006, with respect to claims 7 and 15 have been fully considered and are persuasive. The **102(b) rejections of claims 7 and 15 has been withdrawn.**

4. Applicant's **arguments filed 12 October 2006 regarding the 102(b) rejections of claims 1-6, 8-14 and 16-20 have been fully considered but they are not persuasive.**

i. On page 10 of the remarks, Applicant submits that while Smith discloses adding flip-flops and muxes to the design, Applicant adds a single delay element to each synchronizer. It is noted that the feature upon which applicant relies (i.e., a synchronizer comprised of only a single delay element) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 2 recites a synchronizer that *includes* a first flip-flop and a second flip-flop. This does not preclude adding a multiplexer to the design. The Examiner notes that this argument does not explicitly refer to the rejection of any particular claim.

Regarding the 102(b) rejection of claim 1:

ii. On page 12, Applicant submits that Smith fails to teach the claimed "delay applicator" that applies the random delay to the "first flip-flop" because Smith (figure 2) teaches that

the added delay is applied several flip-flops downstream, not at the first flip-flop as claimed. The Examiner notes that figure 2 shows Smith's invention when used for one cycle, and the Applicant is directed to **figure 5** of the prior art, which shows the invention being used in multiple clock cycles. **Flip-flop 120** in the figure is equivalent to the first flip-flop in the claims, because a **random delay 112** is applied to it, it is clocked by a **first clock 100**, and receives one of the **domain crossing signals generated by the first clock 110** as input.

iii. On pages 12-14, Applicant submits that Smith's delay added by his mux takes on continuous range of values rather than two discrete values. The Applicant is reminded that the claim must be given their broadest reasonable interpretation. See MPEP 2111:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's en banc decision in Phillips v. AWH Corp., 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard: The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359. 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

The claim limitation recites "a delay randomizer that selects as a random delay either a first delay value or a second delay value..." The Applicant appears to be arguing that there are only two possible delays values from which the delay may be selected. However, the Examiner notes that this is not required by the claim language, and asserts that the range of possible delay values disclosed by Smith encompasses the first and second possible delays values claimed.

iv. On page 14, Applicant submits that the difference between the two delays selected by Smith's mux can vary continuously over the range of 0 to 1 clock period, including all the many intermediate values, and therefore Smith teaches away from claim 1's delay randomizer, which claims that the 2 delay values differ by the second clock period. The Applicant is directed to **column 4 lines 59-63** which discloses modifying the signal so that it exhibits an X value, i.e. undetermined *(delaying the signal)* for a period of time at least equal to one clock period relative to the period of clock B *(the second clock)*. Thus, assuming that the Applicant is correct and Smith discloses a plurality of possible delays, he discloses a difference in delay equivalent to the period of the second clock.

Regarding the 102(b) rejection of claim 6:

v. Applicant submits that since Smith produces values that vary all over the map between 0 and 1 clock period, he cannot anticipate claim 6. The Applicant is directed to **column 4 lines 59-63** which discloses modifying the signal so that it exhibits an X value, i.e. undetermined *(delaying the signal)* for a period of time at least equal to one clock period relative to the period of clock B *(the second clock)*. Thus, assuming that the Applicant is correct and Smith discloses a plurality of possible delays, he discloses a difference in delay equivalent to the period of the second clock. As per the Applicant's admission on page 14, Smith produces delay values that vary between zero and a clock period. The latter clock period can be equivalent to the period of Smith's clock B, and thus the Examiner maintains that Smith anticipates claim 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6, 8-14 and 16-20 are rejected under 35 U.S.C. 102(b)** as being clearly anticipated by **Smith et al. (US Patent No. 6,353,906)**, herein referred to as Smith.

Regarding claim 1:

Smith discloses a domain-crossing verifier comprising:

a. a design scanner, receiving a textual design file specifying functions to be performed by a chip being designed, for locating domain-crossing signals generated by a first clock but sampled by a second clock, wherein the first clock and the second clock are asynchronous **(figures 3 and 4; column 3 lines 1-15)**

b. wherein the first clock has a first clock period and the second clock has a second clock period that differs from the first clock period **(figures 3 and 4)**

c. a delay randomizer that randomly selects as a random delay either a first delay value or a second delay value, the first and second delay values substantially differing by the second clock period **(column 4 lines 25-34)**. *The multiplexer encapsulates the functionality of the delay randomizer* because it randomly selects the delay path of the input signal.

d. a delay applicator, coupled to the delay randomizer, for applying the random delay to a first flip-flop, the first flip-flop being clocked by the second clock but receiving one of the domain-crossing signals generated by the first clock as an input **(column 4 lines 25-34)**; *The multiplexer encapsulates the functionality of the delay applicator* because after it randomly selects the delay path of the input signal, it applies this delay to the output signal.

e. wherein the delay applicator applies a series of random delays generated by the delay randomizer to a plurality of the domain-crossing signals located by the design scanner **(column 4 lines 25-34)**

f. wherein the chip defined by the textual design file can be simulated using the random delays that differ by the second clock period to simulate logic hazards caused by domain-crossing signals **(column 4 lines 34-42)**

Regarding claim 2:

Smith discloses the domain-crossing verifier of claim 1 wherein each domain-crossing signal passes through a synchronizer that includes the first flip-flop clocked by the second clock and generating a middle signal, and a second flip-flop that receives the middle signal and is clocked by the second clock to generate a re-synchronized signal that can be sampled by logic in a second domain clocked by the second clock **(figures 2 and 5; column 5 lines 44-67)** and wherein the synchronizers are added to the textual de-sign file by the design scanner or are already part of the textual design file **(column 4 lines 34-42)**

Regarding claims 3 and 4:

Smith discloses the domain-crossing verifier of claim 2 further comprising a cycle simulator, performing the functions defined by the textual design file on input stimuli, the cycle simulator delaying sampling of the domain-crossing signals by the second clock by the random delays generated by the delay randomizer wherein the chip defined by the textual design file is simulated by the cycle simulator using the random de-lays that differ by the second clock period to simulate logic hazards caused by domain-crossing signals **(column 3 lines 56-65; column 4 lines 25-34, 44-63; column 5 lines 44-67)**.

Regarding claim 5:

Smith discloses using a compiler to check for proper syntax and then generating a netlist **(column 1 lines 13-38)**. Smith discloses simulating the HDL design using Cadence, which first compiles the HDL to check for errors and then generates a final netlist.

Regarding claim 6:

Smith discloses the domain-crossing verifier **(column 3 lines 56-65)** of claim 1 wherein the first delay value is zero and the second delay value is the second clock period, or wherein the first delay value is an arbitrary delay value and the second delay value is the arbitrary delay value added to the second clock period **(column 5 lines 56-67; column 6 lines 1-5).**

Regarding claim 7:

Smith discloses the domain-crossing verifier of claim 1 wherein the delay randomizer multiplies a random binary number **(column 4 lines 25-34)** by a period of the second clock to generate the random delay **(column 4 lines 59-67)**. The original signal is delayed *(randomly)* for a period of time at least equal to one clock period relative to the period of clock B *(the second clock)*.

Regarding claim 8:

Smith discloses the domain-crossing verifier of claim 1 wherein the delay randomizer receives a seed value that specifies a starting point in a random-number sequence for generating the random delays **(column 4 lines 33-35)**.

Regarding claim 9:

Smith discloses a method for simulating domain-crossing signals that cross from a first clock domain to a second clock domain comprising:

a. identifying a domain-crossing signal generated by a first clock in the first clock domain, but sampled by a second clock in the second clock domain **(column 5 lines 42)**

b. inserting an added delay to sampling of the domain-crossing signal by the second clock, wherein the added delay is selected from a first delay **(figure 5 delay 106)** and a second delay **(figure 5 delay 110)**, wherein the second delay is a period of the second clock greater than the first delay **(column 5 lines 16-20)** and wherein the steps of identifying a domain-crossing signal and inserting the added delay are repeated for other domain-crossing signals **(figure 6; column 6 lines 11-13)**, wherein some domain-crossing signals have the second delay selected as the added delay while other domain-crossing signals have the first delay selected as the added delay **(column 5 lines 56-67; column 6 lines 1-5)**

c. simulating a design containing the domain-crossing signals having the added delays to sampling by the second clock whereby the design is simulated with added delays on domain-crossing signals wherein the added delays differ by the period of the second clock **(column 2 lines 55-67)**

Regarding claim 10:

Smith discloses the method of claim 9 wherein simulating the design comprises simulating from a design-language file before logic gates are synthesized, whereby domain crossing signals are verified before gate-level syntheses **(column 6 lines 7-15)**. Smith discloses the simulation of the design before gate-level implementation and also discloses implementing the method using a gate-level implementation.

Regarding claim 11:

Smith discloses the method of claim 9, wherein simulating the design comprises simulating from a design language file to verify the domain-crossing signals before layout and wiring **(column 2 lines 55-67)**. The prior art discloses simulating only the circuit model contained in the HDL design, and does not consider the layout and wiring.

Regarding claim 12:

Smith discloses the method of claim 9, wherein the steps of identifying the domain-crossing signals and inserting the added delay are repeated for all domain-crossing signals **(column 2 lines 55-67; column 3 lines 1-15)**. The behavioral synchronization is provided for each synchronization element in the model.

Regarding claims 13 and 14:

Smith discloses the method of claim 12 wherein inserting an added delay comprises randomly selecting the first delay or the second delay as added delay whereby added delays are selected randomly **(column 4 lines 25-28).**

Regarding claim 15:

Smith discloses the method of claim 12 wherein the delay randomizer multiplies a random binary number **(column 4 lines 25-34)** by a period of the second clock to generate the random delay **(column 4 lines 59-67)**. The original signal is delayed *(randomly)* for a period of time at least equal to one clock period relative to the period of clock B *(the second clock)*.

Regarding claim 16:

Smith discloses the method of claim 12 further comprising:

a. inserting a synchronizer onto the domain-crossing signal, wherein the synchronizer comprises a first flip-flop and a second flip-flop in series **(figures 2 and 5; column 2 lines 42-67)**

b. wherein inserting an added delay comprises adding the added delay to an output of the first flip-flop before an input to the second flip-flop, whereby synchronizer delays are randomized **(column 4 lines 25-34).**

Regarding claim 17:

Smith discloses the method of claim 12 wherein the first clock is asynchronous to the second clock **(figures 3 and 4)**.

Regarding claim 18:

Smith discloses the method of claim 12 further comprising:

a. identifying a multi-cycle signal generated by the second clock in the second clock domain **(column 5 lines 5-10)**, wherein the multi-cycle signal is allowed more than one period of the second clock to propagate before being sampled by the second clock **(figures 3 and 4; column 3 lines 16-25)** ;

b. inserting an added delay to sampling of the multi-cycle signal by the second clock **(column 5 lines 61-67)**, wherein the added delay is selected from the first delay and the second delay, wherein the second delay is a period of the second clock greater than the first delay (**column 6 lines 1-5**). *The multiplexer randomly selects the delay and then adds it into the system.*

c. wherein simulating the design includes simulating the multi-cycle signals having the added delays to sampling by the second clock whereby the design is simulated with added delays on multi-cycle signals wherein the added delays differ by the period of the second clock **(column 3 lines 1-25; column 5 lines 61-67; column 6 lines 1-5)**.

Regarding claim 19:

Smith discloses a domain-crossing signal verifier comprising:

a. identifying means for identifying a domain-crossing signal generated by a first clock in a first clock domain, but sampled by a second clock in a second clock domain **(figures 2-5)**; wherein the domain-crossing signal is generated by the first clock passes through a first flip-flop and a second flip-flop in a synchronizer, the first and second flip-flops clocked by the second clock **(column 3 lines 1-15)**

b. delay randomizer means for generating a randomized delay for the first flip-flop in the synchronizer **(column 4 lines 25-42)**, wherein the randomized delay is randomly selected as either a first delay **(figure 5 delay 106)** or a second delay **(figure 5 delay 110)** wherein the second delay is substantially the first delay added to a period of the second clock **(column 5 lines 65-67; column 6 lines 1-5)**;

c. repeat means for activating the delay randomizer means to generate randomized delays for other domain-crossing signals identified by the identifying means **(column 3 lines 1-15)**

d. wherein some domain-crossing signals have the second delay selected as the randomized delay while other domain-crossing signals have the first delay selected as the randomized delay **(column 4 lines 25-42)**

e. simulating means for simulating a design containing the domain-crossing signals having the randomized delays **(column 4 lines 25-42)** for first flip-flops in synchronizers on the domain-crossing signals before sampling by the second clock **(column 5 lines 25-43),** whereby the design is simulated with randomized delays on domain-crossing signals wherein the randomized de-lays differ by the period of the second clock **(column 3 lines 1-15)**

Regarding claim 20:

Smith discloses the domain-crossing signal verifier of claim 19 further comprising multi-cycle means, receiving a list of multi-cycle signals that are allowed more than one period of the second clock for signal propagation, for activating the delay randomizer means to generate randomized delays for a gate in a path of each of the multi-cycle signals on the list of multi-cycle signals;

wherein the randomized delays are applied to multi-cycle signals for simulation by the simulating means **(column 3 lines 1-15; column 4 lines 25-42; column 5 lines 25-43)**.

Allowable Subject Matter

6. Claims 7 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4 January 2007

Shambhavi Patel
Examiner
Art Unit 2128

KAMINI SHAH
SUPERVISORY PATENT EXAMINER